

Claims:

1 1. A quadrature oscillator with phase error correction, comprising:
 2 a local oscillator that generates a single-ended clock signal;
 3 a single-ended to differential converter, coupled to the local oscillator, that
 4 converts the single-ended clock signal to a differential clock signal;
 5 a quadrature generator, coupled to the converter, that converts the differential
 6 clock signal into an in-phase (I) carrier signal and a quadrature (Q) carrier signal;
 7 a phase error detector, coupled to the quadrature generator, that measures a phase
 8 error between the I and Q carrier signals and that provides a phase error signal; and
 9 a feedback amplifier, coupled to the phase error detector and the quadrature
 10 generator, that modifies the differential clock signal based on measured phase error.

1 2. The quadrature oscillator of claim 1, wherein the single-ended to
 2 differential converter includes a second stage that generates a pair of differential clock
 3 signals.

1 3. The quadrature oscillator of claim 1, wherein the quadrature generator
 2 divides the frequency by two.

1 4. The quadrature oscillator of claim 1, wherein the feedback amplifier
 2 applies the measured phase error as a DC offset to an AC differential clock signal.

1 5. The quadrature oscillator of claim 1, further comprising:
 2 the local oscillator asserting the single-ended clock signal as a voltage signal;
 3 the single-ended to differential converter asserting the differential clock signal as
 4 a differential voltage signal;

5 a transconductor, coupled to the single-ended to differential converter and the
6 quadrature generator, that converts the differential clock voltage signal into two pairs of
7 differential current clock signals; and

8 the quadrature generator comprising a master-slave latch configuration, coupled
9 to the transconductor, that generates I and Q current signal outputs from the two pairs of
10 differential current clock signals.

1 6. The quadrature oscillator of claim 5, wherein the transconductor
2 comprises:

3 a dual pair of common-emitter coupled transistors, each pair having a base input
4 receiving a component of the differential clock signal and each pair having a pair of
5 collectors generating a corresponding one of the two pairs of differential current clock
6 signals; and

7 a current source coupled between the emitters of each of the dual pair of
8 transistors and ground.

1 7. The quadrature oscillator of claim 5, further comprising:

2 a first chain of buffers that amplifies the I current signal output to provide the I
3 carrier signal; and

4 a second chain of buffers that amplifies the Q current signal output to provide the
5 Q carrier signal.

1 8. The quadrature oscillator of claim 7, wherein the phase error detector
2 generates a phase error voltage indicative of phase error between the I and Q carrier
3 signals.

1 9. The quadrature oscillator of claim 8, wherein the feedback amplifier
2 comprises:

3 a transconductance stage, coupled to the phase error detector and the quadrature
4 generator, that converts a phase error voltage into a correction current and that adds the
5 correction current to each of the two pairs of differential current clock signals.

1 10. The quadrature oscillator of claim 9, wherein the transconductance stage
2 comprises MOSFET current sources.

3 11. The quadrature oscillator of claim 9, wherein the feedback amplifier
4 further comprises:

5 an RC filter, coupled to the phase error detector; and

6 an amplifier stage, coupled to the RC filter and the transconductor stage, that
7 amplifies the phase error voltage.

1 12. The quadrature oscillator of claim 1, wherein the phase error detector
2 comprises:

3 a first mode buffer, coupled to the quadrature generator, that generates first mode
4 I and Q carrier signals;

5 a second mode buffer, coupled to the quadrature generator, that generates second
6 mode I and Q carrier signals;

7 a first phase error detector that measures a phase error between the first mode I
8 and Q carrier signals and that provides a first mode phase error signal;

9 a second phase error detector that measures a phase error between the second
10 mode I and Q carrier signals and that provides a second mode phase error signal; and

11 a mode switch, coupled to the first and second phase error detectors and the
 12 feedback amplifier, that couples the first phase error detector to the feedback amplifier in
 13 a first mode and that couples the second phase error detector to the feedback amplifier in
 14 a second mode.

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 12 feedback amplifier, that couples the first phase error detector to the feedback amplifier in
 13 a first mode and that couples the second phase error detector to the feedback amplifier in
 14 a second mode.

1 13. A quadrature local oscillator with phase error correction, comprising:

2 a single-ended to differential converter that converts a single-ended clock signal

3 to a differential clock signal;

4 a transconductor, coupled to the single-ended to differential converter, that

5 converts the differential clock signal into a pair of differential clock signals;

6 a quadrature generator, coupled to the transconductor, that converts the pair of

7 differential clock signals into an in-phase (I) clock signal and a quadrature (Q) clock

8 signal;

9 a first chain of buffers, coupled to the quadrature generator, that develops an I

10 carrier signal as a corrected version of the I clock signal, the first chain of buffers having

11 an intermediate feedback junction;

12 a second chain of buffers, coupled to the quadrature generator, that develops a Q

13 carrier signal as a corrected version of the Q clock signal, the second chain of buffers

14 having an intermediate feedback junction;

15 a phase error detector, coupled to the first and second chain of buffers, that

16 measures a phase error between the I and Q carrier signals and that provides a phase error

17 signal;

18 a feedback amplifier, coupled to the phase error detector, that receives the phase

19 error signal and that generates a differential feedback signal; and

20 a pair of tuning elements, each coupled to the feedback amplifier and a respective

21 one of the intermediate feedback junctions of the first and second chain of buffers.

1 14. The quadrature local oscillator of claim 13, wherein each of the pair of

2 tuning elements comprises a tunable RC circuit.

- 1 15. The quadrature local oscillator of claim 13, wherein each of the pair of
2 tuning elements comprises:
3 a series resistance coupled between successive buffers of the chain of buffers; and
4 a tunable varactor coupled to the resistance and the feedback amplifier.

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1 16. A quadrature oscillator with phase error correction, comprising:
 2 a clock generator that provides a clock signal;
 3 a clock splitter, coupled to the clock generator, that splits the clock signal into
 4 first and second clock signals;
 5 a first phase shifting network, coupled to the clock splitter, that develops a first
 6 carrier signal based on the first clock signal;
 7 a second phase shifting network, coupled to the clock splitter, that develops a
 8 second carrier signal based on the second clock signal, wherein the second clock signal
 9 intended to be one quarter phase shifted relative to the first carrier signal; and
 10 a phase detector, coupled to the first and second phase shifting networks, that
 11 asserts a phase error signal used to control the phase shifting networks.

1 17. The quadrature oscillator of claim 16, further comprising:
 2 a combiner, coupled to the phase detector and the clock splitter, that adjusts the
 3 first and second clock signals based on the phase error signal.

1 18. The quadrature oscillator of claim 16, further comprising:
 2 the first and second phase shifting networks each developing a respective one of
 3 first and second intermediate carrier signals; and
 4 a combiner, coupled to the phase detector and the first and second phase shifting
 5 networks, that adjusts the first and second intermediate carrier signals based on the phase
 6 error signal.

1 19. A method of generating quadrature signals with phase error correction,
2 comprising:
3 generating a clock signal;
4 converting the clock signal into a differential clock signal;
5 splitting the clock signal into first and second clock signals;
6 developing an in-phase (I) differential carrier signal and a quadrature phase (Q)
7 differential carrier signal based on the first and second clock signals;
8 detecting phase error between the I and Q differential carrier signals and
9 generating a phase error feedback signal; and
10 adjusting the phase differential between the I and Q differential carrier signals
11 based on the phase error feedback signal.

1 20. The method of claim 19, wherein the adjusting the phase differential
2 comprises combining the phase error feedback signal with the first and second clock
3 signals.

1 21. The method of claim 19, further comprising:
2 generating intermediate I and Q differential carrier signals within a chain of
3 buffers; and
4 the adjusting the phase differential comprises combining the phase error feedback
5 signal with the intermediate I and Q differential carrier signals.